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Remarks

Parts of the office action are not understood. For example, on page 5, the Examiner refers to claim 28, whereas there is currently no claim 28 in the application, as noted on the front page of the office action. Similarly, with regard to the objection to claim 21, the Examiner refers to the language "varied among choices", yet claim 21 contains no such language. It was removed in response to the previous office action and replaced by the more conventional Markush language in claim 21 presently on file. The Examiner is therefore respectfully requested to withdraw the final action and resissue it without such errors.

The objection with respect to the added language Fourier Transform Infrared Spectroscopy is respectfully traversed. **FTIR** is an extremely well known acronym to those skilled in the art. It is so well known that it was believed not to require explanation, especially in view of the Figures, which are clearly FTIR spectra. A simple search for FTIR on the USTPO website revealed 5229 hits. A sample was checked to confirm they relate to Fourier Transform Infrared (not all were checked for practical reasons). A reference to FTIR can be found in the Handbook of Semiconductor Manufacturing Technology, Marcel Decker, Inc., New York ISBN 0-8247-8783-8, published 2000. A copy of page 911 of this publication is attached. The applicants find it difficult to understand why the Examiner does not accept this acronym as a well known term of art. It is so well known that it is respectfully submitted that the Examiner ought to be able to take official notice of its meaning. It is like asking the applicants to provide evidence that °C means degrees Celsius. Or is the Examiner's concern the fact that the word *spectroscopy* has been added. If that is the case, of course, technically the Examiner is correct. FTIR strictly speaking just stands for Fourier Transform Infrared, and claim 20 has been so amended. To provide formal support, but not new matter (since the term is self-explanatory), the acronym has been spelt in full in paragraph 0003.

"in resistant" and cores were typographical error that has been corrected. While the typographical errors are regrettable, it is believed self evident as to what was the intended meaning. Claims 6, 7, 10, 11, 12, 13, and 18 and 19 have been clarified. The structure of course passes through multiple temperatures between the initial and final temperatures. The problem is that it is hard to define a changing temperature in a way that provides a proper antecedent. The

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language of the dependent claims has been amended to make it clear that they relate to limitations on the generic steps defined in claim 1. It is believed that the amended wording solves the problem.

The last part of claim 1 has been clarified. In step f(iii) the temperature is ramped down while the structure undergoes elastic deformation. During this elastic deformation the tensile stress decreases to a final value that is less than the initial value. Paragraph 185 has been corrected. It is clear from Figure 10 that the stress of the core initially increases with temperature and similarly at the final ramp down decreases with temperature.

With regard to claim 21, the dependency was incorrect. Claim 21 should be dependent on claim 20, which provides an antecedent for the various terms specified.

With regard to claim 20, the Examiner has taken a very restrictive view of the term dimensions. It is possible to define a multi-dimensional vector space having a large number of components.

With regard to the objection under 35 USC 103(a), the Examiner notes that "it is unclear how they (the arguments relating to stress level) relate to any claimed limitations" and that features of the specification are not incorporated into the claims. The specification as a whole explains how if the steps explicitly set forth in claim 1 are carried out, the changes in stress level shown in Figure 10 will take place and as a result a high quality component with good absorption characteristics will be obtained. This result follows from the novel sequence of steps set forth in claim 1. If the applicants recite novel steps in a claim, it is permissible to refer the Examiner to the specification to note the advantages that flow from those steps.

It is respectfully submitted that the Examiner has not shown how Ojha allegedly meets the claim limitations with the exception of the cooling step as stated in the office action. For example, with reference to the backside compensating layer, the Examiner refers to col. 3, lines 62-65 of Ohja. These lines read:

> "process time.
>
> BRIEF DESCRIPTION OF THE DRAWINGS
>
> Arrangements illustrative of the invention will now be ..."

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It appears the Examiner has misquoted the passage, but even allowing for that the applicants are unable to find any reference to a compensating layer on the backside of the wafer. The wafer in Ohja is clearly indicated as 13 (see Figure 1). In semiconductor usage a wafer has a clear and distinct meaning. A wafer is a substrate onto which layers may be deposited. It is not in itself a deposited layer. It is defined in the McGraw Hill Dictionary of Scientific and Technical terms (fifth edition) as "a thin semiconductor slice on which matrices of microcircuits can be fabricated". Language has to be interpreted in accordance with its natural meaning unless there is any indication that a meaning other than the natural meaning is intended. There is absolutely no teaching in Ohja (that the applicants can find) of a layer that is deposited on the backside of the wafer to make the waver resistant to warp during subsequent processing. Moreover, there would be on reason to include a backside compensating layer in Ohja (without the benefit of the teachings of the present invention) since there is no discussion in Ohja of wafer bow or any suggestion that this a potential problem.

In the absence of a correct indication of why the Examiner believes Ohja discloses the deposition of buffer layers on the front and backside of wafer 13 (when in the applicants respectful submission this is evidently clearly not the case), it is very difficult for the applicants to know what case they have to answer. Indeed since this is such crucial part of the claim, and the Examiner's citation is clearly incorrect, if the Examiner still maintains his position, it is respectfully submitted that he should withdraw the final action and reissue it with the correct citation so that the applicant can properly know what case he has to answer.

Step *a* of claim 1 requires depositing silica buffer layers respectively on a front and back face of a silicon wafer by PECVD (Plasma Enhanced Chemical Vapor Deposition) to provide a first structure resistant to wafer warp during thermal processing. In Ohja, not only is item 13 is clearly identified as the wafer, item 13 is clearly consistent with the meaning of *wafer* as understood by persons skilled in the art. No compensating layer is deposited on the backside of this wafer, so clearly this step is absent.

Steps *b* and *c* define a specific treatment that is applied to the structure resulting from step a, but since step *a* is absent these steps cannot be present either.

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Step *d* requires the deposition of a core layer on the first structure after undergoing the treatment set forth in steps *b* and *c*.

Step *f* then recites the thermal treatment to which the second structure is subject.

Ohja doesn't' even teach anything about subjecting any structure, let alone one with buffer layers on both sides of a wafer, to a heat treatment remotely related to the present invention. Ohja teaches annealing the *cladding* layer (for reasons totally unrelated to the present invention), which inherently is deposited after the core layer. For example, see the paragraph commencing at line 45, col. 3, where Ohja states that "The required cladding layer thickness may be provided by a number of separate depositions stages, each deposited layer being separately annealed."

In conclusion, Ohja to the extent that it discloses annealing one or more cladding layers, which inherently are all on the same side of the wafer, is not remotely close, even when the language is stretched to breaking point, to the present invention. It teaches annealing for the purpose of removing impurities in the cladding layer; it does not teach depositing buffer layers on opposite sides of a wafer to form a first structure, heat treating the first structure in the manner claimed, depositing a core layer on the buffer layer on the front face of the wafer, and then heat treating the second structure in the manner claimed.

While the terms wafer, buffer, core and cladding have well known meanings in the art, even if the Examiner disregards such meanings, it would make no sense to consider the wafer 13 a "buffer layer" deposited on the buffer layer 12. You cannot deposit a substrate onto a deposited layer.

It is believed that Ohja is so remote from the invention claimed that the invention is patentable. However, if the Examiner wishes to maintain his objections, he is respectfully requested to point out for the purposes of appeal exactly how he believes the teachings of Ohja meet the claim limitations set forth in the light of the above discussion. It is respectfully submitted that it is not apparent from the office action, especially in view of the incorrectly cited passage, how the Examiner believes Ohja meets the claim limitations including the buffer layer deposited on the backside of the wafer.

Reconsideration and allowance are therefore respectfully requested.

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